BU-63155L3

MIL-STD-1553 DATA BUS +5.0 VOLT SINGLE TRANSCEIVER

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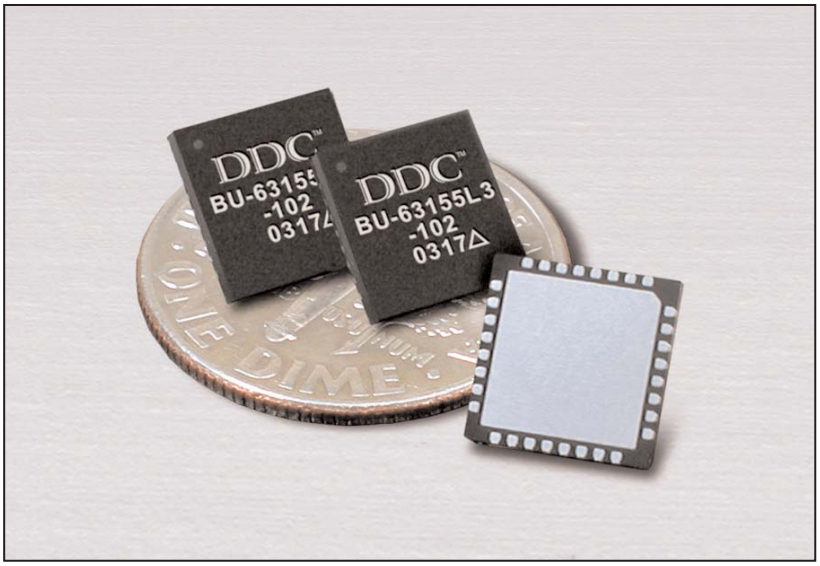

FEATURES

- World's Smallest +5.0V MIL-STD-1553 Transceiver
- -55°C to +125°C Operation
- 0.28 x 0.28" (7 X 7 mm) Body and Footprint Size
- Requires Only +5.0V Power Supply
- Low Power Consumption
- 32-Pad LPCC Package
- 0.040" (1 mm) Maximum Height
- Single Transceiver Allows Full Dual Redundancy

DESCRIPTION

The BU-63155 transceiver is a complete transmitter and receiver fully conforming to MIL-STD-1553A, 1553B, and 1760. The use of two BU-63155 Transceivers provides full dual redundancy. Features include: +5.0V power supply voltage, Harris interface type, and an ultra low profile, small footprint, 32-pad Leadless Plastic Chip Carrier package (LPCC). The LPCC package provides an integral, exposed heatsink on the package bottom. This package allows 100% duty cycle operation at 125°C when the heatsink is soldered to an appropriately constructed PCB.

The receiver section of the BU-63155 accepts Manchester II data from a MIL-STD-1553 Data Bus and produces TTL level signals at its outputs: RX DATA OUT and $\overline{\text{RX DATA OUT}}$. These outputs represent positive and negative excursions of the input data signals beyond an internally fixed threshold level. An external STROBE input enables or disables the receiver's outputs.

The transmitter section accepts bipolar TTL signal data at its TX DATA IN and $\overline{\text{TX DATA IN}}$ inputs and produces Manchester II data at the TX DATA OUT and $\overline{\text{TX DATA OUT}}$ outputs.

When used with the recommended transformers, the transmitter typically produces 21.5Vp-p for transformer coupled outputs and 7.5Vp-p at the bus. An external input, TX INHIBIT, takes priority over the transmitter inputs and disables the transmitter when activated with a logic "1". The ultra small size, +5.0V power supply voltage, and compliance with MIL-STD-1553A, 1553B, and 1760 simplify engineering design, making it an excellent choice for interfacing with any MIL-STD-1553 system.

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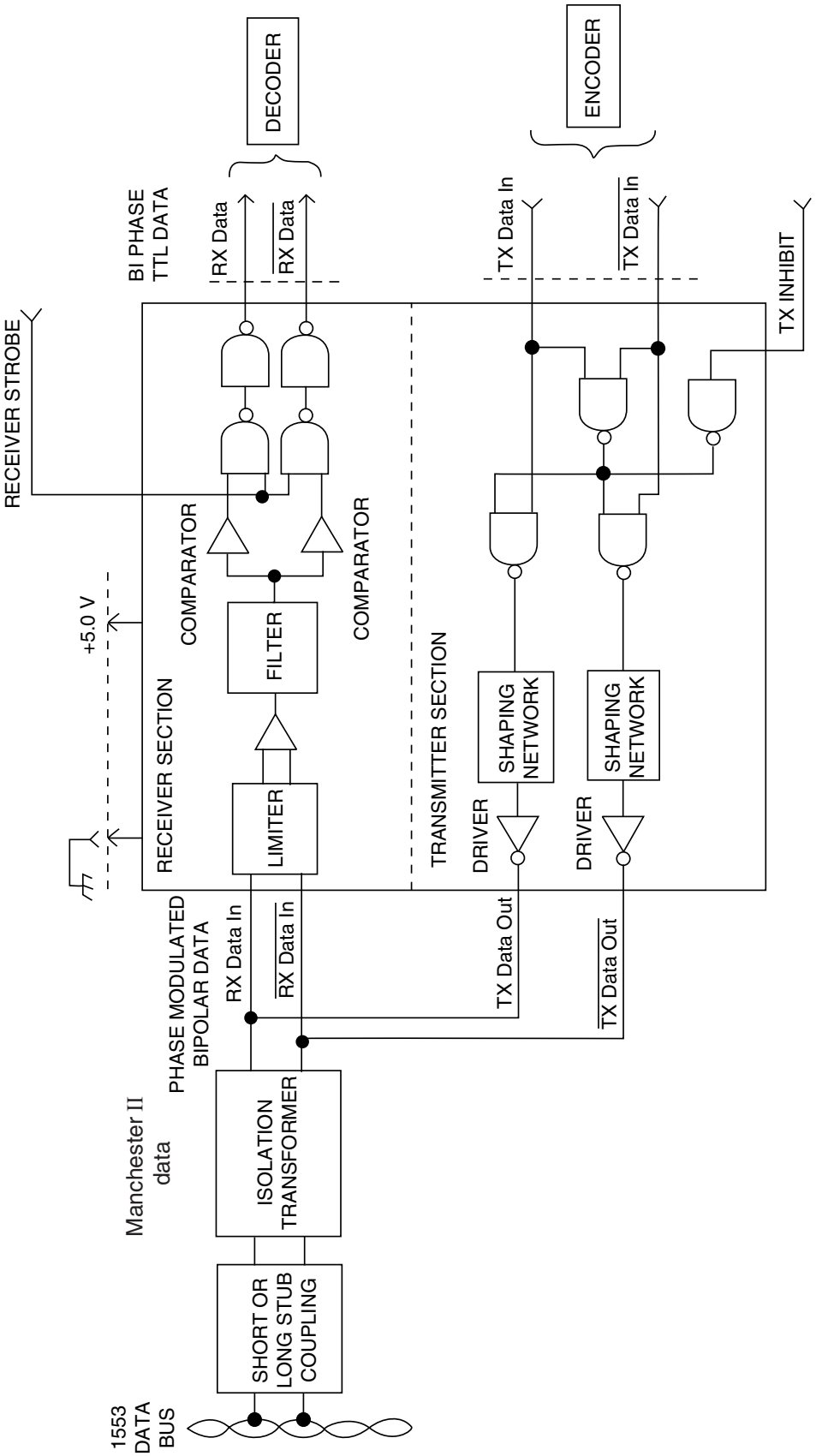


FIGURE 1. BU-63155L3 BLOCK DIAGRAM

TABLE 1. BU-63155L3 SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
ABSOLUTE MAXIMUM RATINGS				
Supply Voltage				
+5.0 V	-0.3	5.0	7.0	Vdc
RECEIVER				
Differential Input Resistance (Notes 1-6, 12)	2.5			kOhm
Differential Input Capacitance (Notes 1-6, 12)			25	pF
Threshold voltage, transformer Coupled, Measured on Stub (Note 7)	0.200		0.860	Vp-p
Common-Mode Voltage (Note 8)			10	Vpeak
RX DATA (or $\overline{\text{RX DATA}}$) Rise time, Vin 1.2 Vpp			20	ns
RX DATA (or $\overline{\text{RX DATA}}$) Fall time, Vin 1.2 Vpp			20	ns
RX DATA (or $\overline{\text{RX DATA}}$) Rise time, Vin 9.0 Vpp			20	ns
RX DATA (or $\overline{\text{RX DATA}}$) Fall time, Vin 9.0 Vpp			20	ns
RX DATA IN/$\overline{\text{RX DATA IN}}$ to RX DATA/$\overline{\text{RX DATA}}$ delay time			450	ns
RX DATA (or $\overline{\text{RX DATA}}$) STROBE delay (Active to Inhibit OR Inhibit to Active)			100	ns
TRANSMITTER				
Differential Output Voltage				
Direct Coupled Across 35 Ohm, measured on bus	6	7.2	9	Vp-p
Transformer Coupled Across 70 Ohm, measured on Stub (Note 9)	20	21.5	27	Vp-p
Output Noise, differential (Direct coupled)			10	mVp-p
Output Offset Voltage, transformer Coupled Across 70 Ohm	-250		250	mVp
Rise/Fall Time	100	150	300	ns
TX DATA IN/$\overline{\text{TX DATA IN}}$ to TX DATA OUT/$\overline{\text{TX DATA OUT}}$ delay time			250	ns
TX INHIBIT delay (Inhibit to Active)			250	ns
TX INHIBIT delay (Active to Inhibit)			400	ns
LOGIC				
V_{IH}	2.0		Vcc	V
V_{IL}	0		0.8	V
I_{IH} (TX DATA IN, $\overline{\text{TX DATA IN}}$, TX INHIBIT)	20		100	µA
I_{IH} (STROBE)			0	µA
I_{IL} (TX DATA IN, $\overline{\text{TX DATA IN}}$, TX INHIBIT)	0			µA
I_{IL} (STROBE)	-100		-20	µA
V_{OH} (V_{CC} = 4.75V, I_{OH}=max)	4.0			V
V_{OL} (V_{CC} = 4.75V, I_{OL}=min)			0.4	V
I_{OL}	4.0			mA
I_{OH}			-2.4	mA
POWER SUPPLY REQUIREMENTS				
Voltages/Tolerance				
+5.0V	4.75	5.0	5.25	Vdc
Current Drain (Note 10)				
• Idle		40	50	mA
• 25% Duty Transmitter Cycle		166	200	mA
• 50% Duty Transmitter Cycle		280	330	mA
• 100% Duty Transmitter Cycle		480	550	mA
POWER DISSIPATION, Vcc = 5.0V (NOTE 10)				
• Idle		0.20	0.25	W
• 25% Duty Transmitter Cycle		0.48	0.65	W
• 50% Duty Transmitter Cycle		0.70	0.95	W
• 100% Duty Transmitter Cycle		1.00	1.35	W
THERMAL				
Thermal Resistance, Junction-to-Heatsink		7	9	°C/W
Thermal Resistance, Junction-to-Board (Note 11)		14	17	°C/W
Heat sink soldered to PC board (2s2p - JESD51-5)				
Operating Case Bottom Temperature	-55		+125	°C
Operating Junction Temperature	-55		+150	°C
Storage Temperature	-65		+150	°C
Pad Temperature (soldering, 10 sec.)			+300	°C
PHYSICAL CHARACTERISTICS				
Moisture Sensitivity Level		MSL-2		—
Package Body Size (Maximum)		0.280 X 0.280 X 0.040 MAX		in.
32-pad LPCC		(7.1 x 7.1 x 1.0)		(mm)
Weight		0.0049		oz
		(0.14)		(g)

Notes 1 through 6 and 12 are applicable to the Receiver Differential Resistance and Differential Capacitance specifications:
(1) Specifications include both transmitter and receiver (assumed tied together externally without a transformer).

TABLE 1 Notes (Continued):
(2) Impedance parameters are specified directly between pads Tx Data Out / RX Data In and $\overline{\text{Tx Data Out}}$ / $\overline{\text{RX Data In}}$ of the package.
(3) It is assumed that all power and ground inputs to the package are connected.
(4) The specifications are applicable for both un-powered and powered conditions.
(5) The specifications assume a 1.5-volt rms balanced differential, sinusoidal input. The applicable frequency range is 75 kHz to 1 MHz.
(6) Minimum resistance and maximum capacitance parameters are guaranteed over the operating range, but are not tested.
(7) The Threshold Level, as referred to in this specification, is meant to be the maximum peak-to-peak voltage (measured on the stub) that can be applied to the receiver's input without causing the output to change from the OFF state.
(8) Assumes a common-mode voltage within the frequency range of dc to 2 MHz, applied to pins of the isolation transformer on the stub side (either direct or transformer coupled), and referenced to hybrid ground. Transformer must be a DDC recommended transformer.
(9) MIL-STD-1760 requires minimum output voltage of 20Vp-p on the stub connection.
(10) Current drain and power dissipation specifications are preliminary and subject to change. Power dissipation specifications assume a transformer coupled configuration with external dissipation (while transmitting with 100% duty cycle) of 1.4W (for 1760 amplitudes), which is the power delivered to the 1553 fault isolation resistors, the power delivered to the bus termination resistors, the copper losses in the transceiver isolation transformer and the bus coupling transformer.
(11) Thermal resistance specs are preliminary and subject to change. Junction-to-board thermal resistance is measured in accordance with JEDEC standard JESD51-8. The 16 thermal vias connecting the LPCC heatsink to PCB internal plane are in accordance with JEDEC JESD51-5 (2s2p). Each via is 0.3 mm diameter with 0.035 mm plating. Please refer to JEDEC standard JESD51-5 for detailed PCB construction.
(12) To calculate the loading effect on the stub side of the "long stub" isolation transformer, multiply "R" by 3.20 (Isolation Transformer ratio of 1.79^2) and divide "C" by 3.20. For "short stub" isolation transformers, multiply "R" by 6.25 (Isolation Transformer ratio of 2.50^2) and divide "C" by 6.25.

INTRODUCTION

The BU-63155L3 is a single transmitter and receiver packaged in a 32-pad LPCC. It is directly compatible to the Harris 15530 encoder/decoder and has internal (factory preset) threshold levels. The transceiver only requires +5V power and conforms to MIL-STD-1553A and 1553B.

FIGURE 3 illustrates the connection between a BU-63155L3 transceiver and a MIL-STD-1553 Data Bus. After transformer isolating the transceiver, it can be either direct coupled (short stub) or transformer coupled (long stub) to the Data Bus.

TRANSMIT OPERATING MODE

The transmitter section accepts encoded TTL data and converts it to bi-phase Manchester II form using a waveshaping network and driver circuits. The driver outputs TX DATA OUT and $\overline{\text{TX DATA OUT}}$ are transformer coupled to the Data Bus.

The transmitter output terminals can be put into a high impedance state by setting TX INHIBIT high, or setting TX DATA IN and $\overline{\text{TX DATA IN}}$ to the same logic level.

RECEIVER OPERATING MODE

The receiver section accepts data from a MIL-STD-1553 Data Bus when coupled to the Data Bus as shown in FIGURE 3. This data is converted to TTL and furnished to RX DATA OUT and $\overline{\text{RX DATA OUT}}$.

When STROBE is high data passes through the receiver to RX DATA OUT and $\overline{\text{RX DATA OUT}}$. Applying a low to STROBE disables the receiver output terminals.

As illustrated in FIGURE 2, the receiver in the BU-63155L3 provides compatibility to the Harris type decoder.

WAVEFORMS

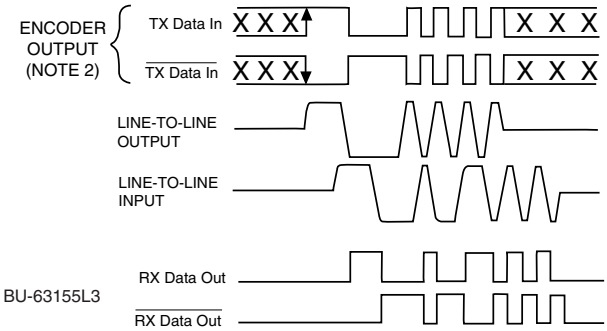
FIGURE 2 illustrates the BU-63155L3 with Harris type decoder interface. Note that TX DATA IN and $\overline{\text{TX DATA IN}}$ inputs must be complementary waveforms with a 50% duty cycle.

1553 BUS INTERFACE AND LAYOUT CONSIDERATIONS

FIGURE 3 illustrates the interface between the BU-63155L3 and a MIL-STD-1553 bus. Connections for direct (short stub) and transformer (long stub) coupling, as well as typical peak-to-peak voltage levels at various points (when transmitting), are indicated in the diagram.

Note that the BU-63155L3 has multiple pads for each of the TX DATA OUT phases. All pads of the same signal phase must be connected together on the PCB to assure adequate current carrying capacity.

The center tap of the primary winding (the side of the transformer that connects to the BU-63155L3) must be directly connected to the ground plane.



Notes:
(1) TX Data In and RX Data Out are TTL signals.
(2) TX Data In inputs must be at the same logic level when not transmitting.
(3) LINE-TO-LINE output voltage is measured between TX Data Out and $\overline{\text{TX Data Out}}$.
(4) LINE-TO-LINE input voltage is measured on the Data Bus.

FIGURE 2. WAVEFORMS FOR HARRIS TYPE ENCODER/DECODER

Furthermore, when transmitting, large currents will flow from the 5V plane, into the LPCC package Vcc pads, out through the TX DATA OUT / $\overline{\text{TX DATA OUT}}$ pads, through the transformer primaries and then out through the center tap and into the ground plane. The traces in this path should be sized accordingly and the connections to the 5V and ground planes should be as short as possible. Note that the heatsink on the bottom of the package is also electrically grounded.

It is recommend that the BU-63155L3 be bypassed with a 10 µF low inductance tantalum capacitor in parallel with a 0.01µF ceramic capacitor. These capacitors should be located as close to the Vcc and GND pads as possible.

To achieve its full military temperature range rating, the BU-63155L3 needs to be properly heat sinked. The thermal resistance junction-to-board specification (TABLE 1) allows for 16 thermal vias connecting the heatsink on the package bottom to a 2s2p (2 sided, 2 plane PCB), 3.0" x 4.5". The thermal via construction follows JEDEC standard JESD51-5 with thermal vias connecting the top side mini-plane located under the heatsink to the upper internal plane. The board temperature is determined 1 mm from the package in accordance with JEDEC standard JESD51-8.

The 2s2p PCB construction has 2 inner planes of 1 oz copper, 2 outer trace layers of 2 oz copper and has an overall thickness of 1.6 mm, which is divided evenly amongst the 3 dielectrics. The top layer has 8 traces (0.26 mm width each) fanning out from each side of the package. Refer to the appropriate JEDEC standards, and DDC's Application Note AN/B-39 "MIL-STD-1553 LPCC PACKAGED TRANSCEIVERS, A USER'S GUIDE" for further information.

ISOLATION TRANSFORMERS

In selecting isolation transformers to be used with the BU-63155L3, there is a limitation on the maximum amount of leakage inductance. If this limit is exceeded, the transmitter rise and fall times may increase, possibly causing the bus amplitude to fall below the minimum level required by MIL-STD-1553. In addition, an excessive leakage imbalance may result in a transformer dynamic offset that exceeds 1553 specifications.

The maximum allowable leakage inductance is 6.0 µH, and is measured as follows:

The side of the transformer that connects to the BU-63155L3 is defined as the "primary" winding. If one side of the primary is shorted to the primary center-tap, the inductance should be measured across the "secondary" (transformer coupled) winding. This inductance must be less than 6.0 µH. Similarly, if the other side of the primary is shorted to the primary center-tap, the inductance measured across the "secondary" (transformer coupled) winding must also be less than 6.0 µH.

The difference between these two measurements is the "differential" leakage inductance. This value must be less than 1.0 µH. Beta Transformer Technology Corporation (BTTC), a subsidiary of DDC, manufactures transformers in a variety of mechanical configurations with the required turns ratios of 1:2.5 direct coupled, and 1:1.79 transformer coupled. TABLE 2 provides a listing of these transformers.

For further information, contact BTTC at 631-244-7393 or at www.bttc-beta.com.

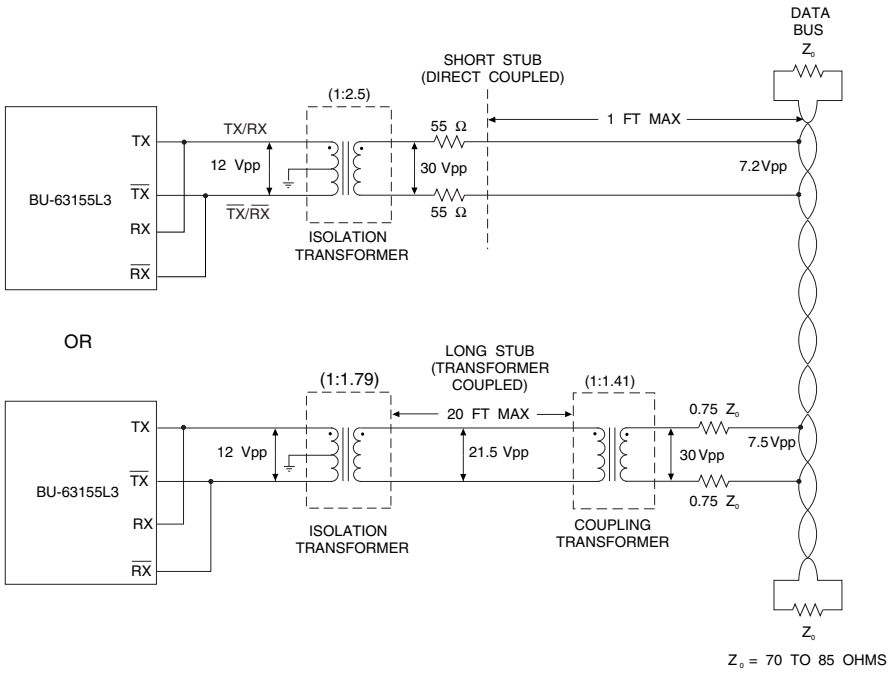


FIGURE 3. BU-63155L3 INTERFACE TO A MIL-STD-1553 BUS

TABLE 2. BTTC TRANSFORMERS FOR USE WITH BU-63155L3		
TRANSFORMER CONFIGURATION	**DIMENSIONS (INCHES)**	**BTTC PART NUMBER**
Single epoxy transformer, through-hole	0.625" X 0.625", 0.250" max height	B-3067, B-3226
Single epoxy transformer, through-hole with stand-offs	0.625" X 0.625", 0.275" max height	B-3225
Single epoxy transformer, surface mount	0.625" X 0.625", 0.275" max height	B-3227
Single epoxy transformer, through-hole	0.350" X 0.500", 0.250" max height	B-3229, B-3230
Single epoxy transformer, flat pack	0.625" X 0.625", 0.275" max height	B-3231
Single epoxy transformer, through-hole	0.625" X 0.625", 0.220" max height.	B-3818
Single epoxy transformer, surface mount	0.625" X 0.625", 0.220" max height	B-3819
Single epoxy transformer, flat pack	0.625" X 0.625", 0.220" max height	B-3820
Single epoxy transformer, flat pack	0.625" X 0.625", 0.150" max height	LPB-5014
Single epoxy transformer, surface mount	0.625" X 0.625", 0.150" max height	LPB-5015
Dual epoxy transformer, twin stacked, through hole	0.625" X 0.625", 0.320" max height	TST-9107
Dual epoxy transformer, twin stacked, surface mount	0.625" X 0.625", 0.320" max height	TST-9117
Dual epoxy transformer, twin stacked, flat pack	0.625" X 0.625", 0.320" max height	TST-9127
Dual epoxy transformer, twin stacked, through hole	0.625" X 0.625", 0.280" max height	TST-9007
Dual epoxy transformer, twin stacked, surface mount	0.625" X 0.625", 0.280" max height	TST-9017
Dual epoxy transformer, twin stacked, flat pack	0.625" X 0.625", 0.280" max height	TST-9027
Dual epoxy transformer, side-by-side, through-hole	0.930" X 0.630", 0.155" max height	TLP-1205, B-3300
Dual epoxy transformer, side-by-side, flat pack	0.930" X 0.630", 0.155" max height	TLP-1105, B-3261
Dual epoxy transformer, side-by-side, surface mount	0.930" X 0.630", 0.155" max height	TLP-1005, B-3310
Single epoxy transformer, flat pack	0.750" X 0.750", 0.130" max height	SLP-8124 (see Note 1)
Single epoxy transformer, surface mount	0.750" X 0.750", 0.130" max height	SLP-8107 (see Note 1)
Dual epoxy transformer, side-by-side, flat pack	1.410" X 0.750", 0.130" max height	DLP-7114 (see Note 1)
Dual epoxy transformer, side-by-side, surface mount	1.410" X 0.750", 0.130" max height	DLP-7115 (see Note 1)
Single nickel-plated kovar transformer, flat pack	0.630" X 0.630", 0.175" max height	HLP-6014
Single nickel-plated kovar transformer, surface mount	0.630" X 0.630", 0.175" max height	HLP-6015
Single epoxy transformer, surface mount	0.400" X 0.400", 0.185" max height	MLP-2005 (see Note 1)
Single epoxy transformer, surface mount	0.400" X 0.400", 0.185" max height	MLP-2205 (see Note 1)
Single epoxy transformer, surface mount	0.400" X 0.400", 0.260" max height	MMT-3005
Single epoxy transformer, surface mount	0.400" X 0.400", 0.260" max height	MMT-3205

Note:
1. Operates to +105°C max. All other transformers operate to +130°C max.

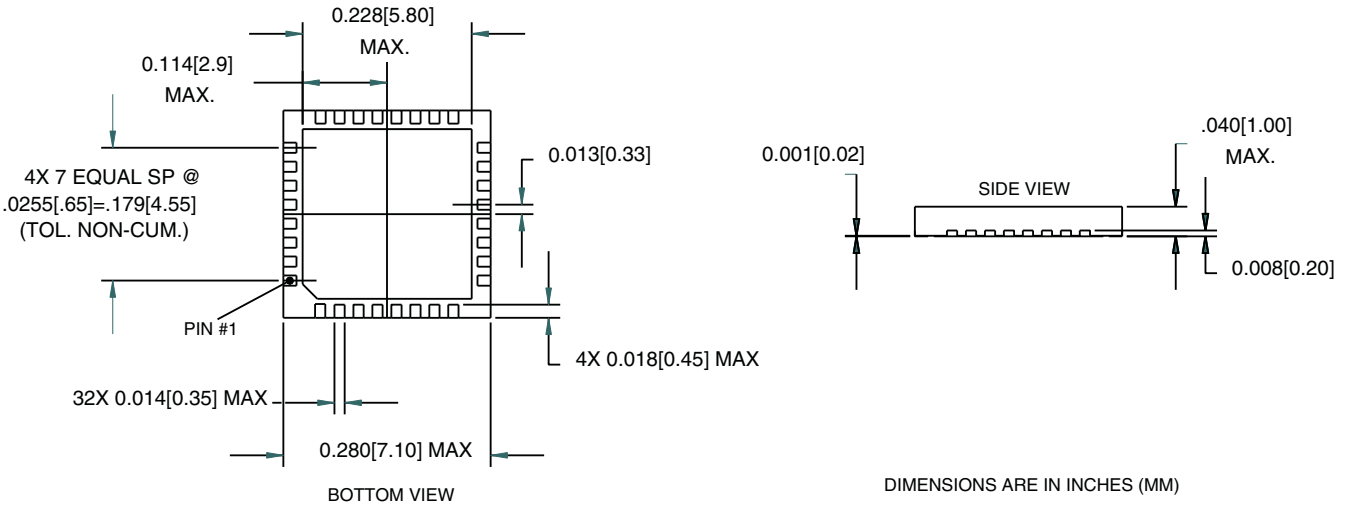


FIGURE 4. BU-63155 MECHANICAL OUTLINE

TABLE 3. BU-63155 PAD & SIGNAL DESCRIPTIONS		
PAD NUMBER	NAME	DESCRIPTION
1	GROUND	Ground
2	Factory Test Point	No connection
3	Factory Test Point	No connection
4	Factory Test Point	No connection
5	Factory Test Point	No connection
6	GROUND	Ground
7	V_{CC}	+5.0 volt power in
8	RX DATA	Receiver output
9	STROBE	Receiver strobe (input)
10	$\overline{\text{RX DATA}}$	Inverted receiver output
11	Factory Test Point	No connection
12	GROUND	Ground
13	V_{CC}	+5.0 volt power in
14	V_{CC}	+5.0 volt power in
15	GROUND	Ground
16	GROUND	Ground
17	RX DATA IN	Receiver input
18	$\overline{\text{RX DATA IN}}$	Inverted receiver input
19	Factory Test Point	No connection
20	V_{CC}	+5.0 volt power in
21	RESERVED	No connection
22	TX INHIBIT	Transmitter Inhibit
23	TX DATA IN	Transmitter input
24	$\overline{\text{TX DATA IN}}$	Inverted transmitter input
25	GROUND	Ground
26	TX DATA OUT	Transmitter output
27	TX DATA OUT	Transmitter output
28	V_{CC}	+5.0 volt power in
29	V_{CC}	+5.0 volt power in
30	$\overline{\text{TX DATA OUT}}$	Inverted transmitter output
31	$\overline{\text{TX DATA OUT}}$	Inverted transmitter output
32	Factory Test Point	No connection
Heatsink	GROUND	Ground

Note:
1. The heatsink on the package bottom is electrically grounded. Connect all pads of each of the Tx-Data Out phases together to ensure sufficient current carrying capacity.

BU-63155 L 3 - 1 0 2

Test Criteria:
2 = MIL-STD-1760 Amplitude Compliant

Process Requirements:
0 = Standard DDC Processing, no Burn-In

Temperature Grade/Data Requirements:
1 = -55°C to +125°C

Voltage/Transceiver Option:
3 = +5.0 volt, rise/fall times = 100 to 300 ns (-1553B)

Package Type:
L = 32-Pad Leadless Plastic Chip Carrier

Product Type:
BU-63155 = Single +5.0V Plastic LPCC Transceiver

Note: 1) The above products contain tin-lead solder finish as applicable to solder dip requirements.

STANDARD DDC PROCESSING FOR PLASTIC MONOLITHIC PRODUCTS		
TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION / WORKMANSHIP	2017	—
ELECTRICAL TEST	DDC ATP	—

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