

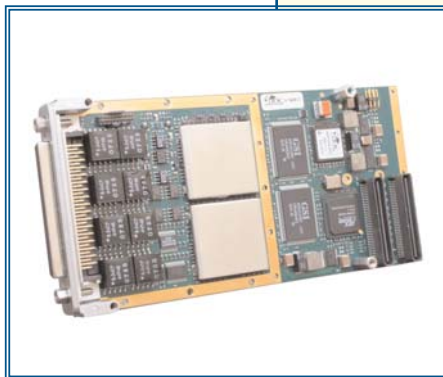
# EIGHT CHANNEL MIL-STD-1553 PMC CARD DATA SHEET



MODEL: BU-65578F/M

## FEATURES

- Conduction or Air Cooled PMC
- Front or Rear I/O
- Configuration with up to:
  - 8 Dual Redundant 1553 Channels
  - 8 Digital Discrete I/O's
  - 8 Avionics (+35V) Discrete I/O's
- IRIG-B Time Code Input
- IRIG-B Time Code Out/Generator
- External Time Tag Clock Input
- External Time Tag Clock Output
- IRIG-106 Chapter 10 Monitor
- E<sup>2</sup>MA BC/RT/MT Architecture
  - API compatible with DDC's Enhanced Mini-ACE BU-69090S Library Software
- 1 MB RAM w/parity per Channel
- Built In Self Test
- 48-bit / 1 $\mu$ s Time Stamp
- Support for VxWorks®, Linux® & Windows® 2000/XP



## DESCRIPTION

The BU-65578F/M is a PMC card that provides up to eight dual-redundant MIL-STD-1553 channels operating in BC, RT, MT, or combined RT/MT modes. The card also contains up to eight digital discrete I/Os, eight avionics (+35V) discrete I/Os, an IRIG-B time code input, an IRIG-B time code output/generator, an external time tag input, and an external time tag clock output.

The MIL-STD-1553 interface used on this card is DDC's Extended Enhanced Mini-ACE® (E<sup>2</sup>MA) architecture which is fully API compatible with the industry standard, field proven, Enhanced Mini-ACE software. The card includes the BU-69092S MIL-STD-1553 Enhanced Mini-ACE (EMACE) Plus C Software Development Kit (SDK) along with source code samples, and detailed documentation.

Each channel is individually configurable as a Bus Controller (BC), Remote Terminal (RT), Bus Monitor (MT) or combined RT / Monitor. The advanced BC architecture provides a high degree of flexibility and autonomy by improving message schedule control, minimizing host overhead for asynchronous message insertion, facilitating bulk data transfers, double buffering, message retry, bus switching strategies, data logging, and fault reporting. The RT architecture provides flexibility in meeting all MIL-STD-1553B protocols. The card has an intelligent hardware offload DMA architecture that dramatically reduces PCI bus and host CPU utilization while storing 1553 monitor data in a convenient and portable IRIG-106 Chapter 10 file format. The card includes the MIL-STD-1553 Enhanced Mini-ACE (EMACE) Plus C Software Development Kit (SDK) and drivers to support all modes of operation in Linux 2.6.x, VxWorks 5.x/6.x and Windows 2000/XP, including source code samples and detailed documentation.

## APPLICATIONS

The card's rugged construction and ability to operate from -40°C to +85°C make it ideal for use in mission computers, flight data recorders, displays, ground vehicles, and other embedded systems that require a military-grade card. The card can be ordered with front or rear I/O and can be used in conduction- or air-cooled applications. The card is a valuable addition to design and test teams involved with MIL-STD-1553 interfaces.

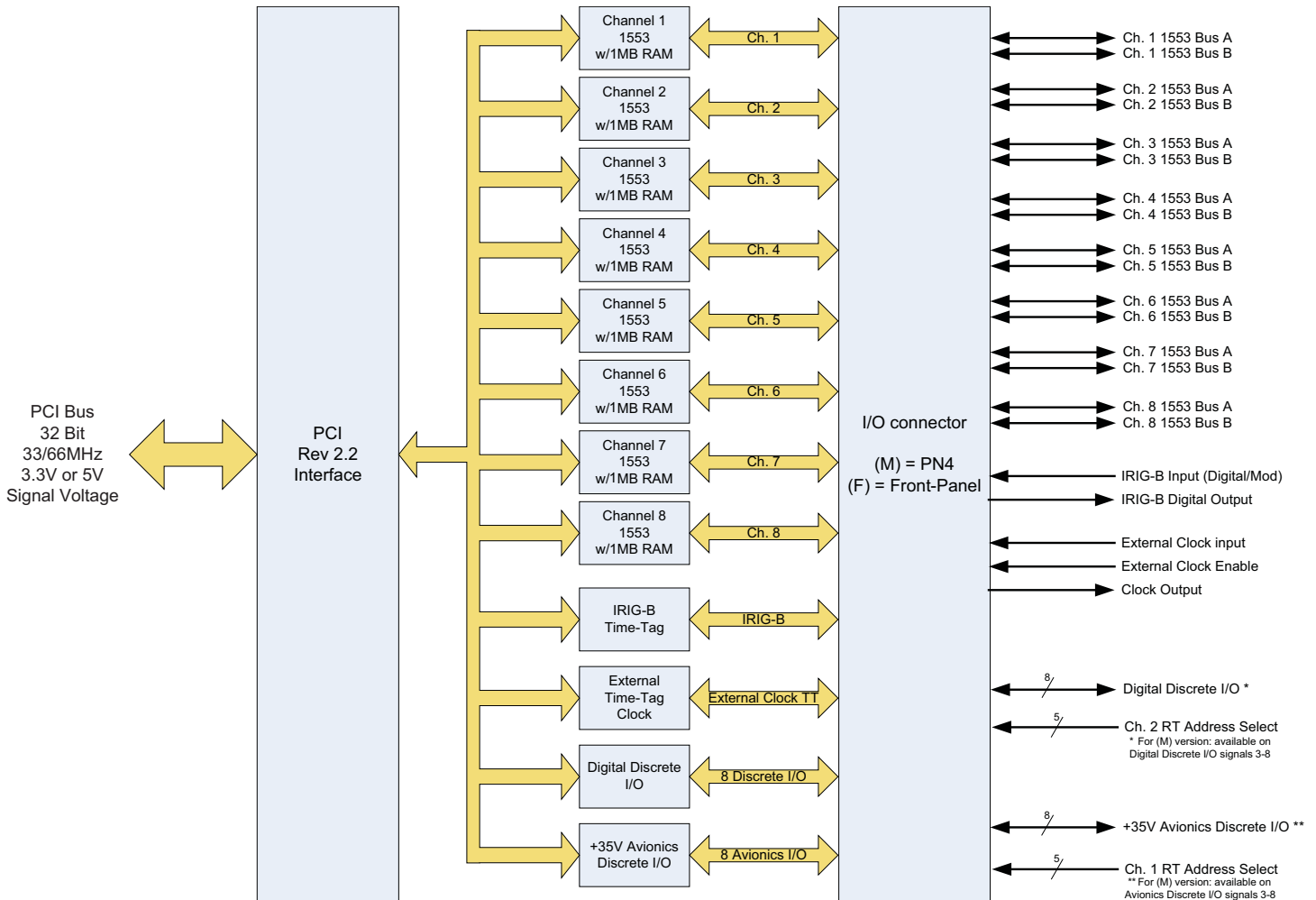
Make Sure the next Card<sup>®</sup>  
you purchase has...



# Quick Specifications

PARAMETER	MIN	TYP	MAX	UNITS	PARAMETER	MIN	TYP	MAX	UNITS
<b>ABSOLUTE MAXIMUM RATINGS</b>					<b>THERMAL</b>				
Supply Voltage +5V	-0.3		6.0	V	Operating Temperature <b>BU-65578F/Mx-2A0</b> (measured at component case) +71°C inlet air temperature with 5 CFM airflow @ 100% duty cycle on all 8 channels	-40		+85	°C
<b>POWER SUPPLY REQUIREMENTS</b>					<b>BU-65578F/Mx-2C0</b> (measured at thermal rail)				
Voltages/Tolerance +5V	4.75	5.0	5.25	V	<b>BU-65578F/Mx-3L0</b> (ambient)	0		+71	°C
<b>CURRENT DRAIN</b>					<b>Storage Temperature</b>				
<b>BU-65578F/M1</b> 0% Transmit / Monitor 75% Transmitter Duty Cycle		340	380	mA		-65		+150	°C
		640	710	mA					
<b>BU-65578F/M2</b> 0% Transmit / Monitor 75% Transmitter Duty Cycle		350	390	mA	<b>PHYSICAL CHARACTERISTICS</b>				
		.92	1.0	A	<b>Weight</b> BU-65578F/M8		4.80		oz.
<b>BU-65578F/M4</b> 0% Transmit / Monitor 75% Transmitter Duty Cycle		360	400	mA			136		(g)
		1.4	1.6	A	<b>Note:</b> For full specifications and additional information refer to the <i><b>BU-65578FM Hardware Manual</b></i> (#MN-65578FX-001) and the <i><b>BU-69092 EMACE Plus SDK Software Manual</b></i> (#MN-69092SX-001).				
<b>BU-65578F/M8</b> 0% Transmit / Monitor 75% Transmitter Duty Cycle		530	600	mA					
		2.7	2.9	A					

**Figure 1. BU-65578F/M Block Diagram**



## MIL-STD-1553 CHANNELS

Each MIL-STD-1553 channel can emulate a Bus Controller (BC), a Remote Terminal (RT), a Bus Monitor (MT), or a combined RT/MT. Standard features include 1MB of RAM with parity per channel, 48-bit message time tagging, IRIG-B time code input, IRIG-B time code output, transformer coupling, triggers, extensive BC & RT frame structures, error detection, RT Status Bit and Mode Code responses, along with advanced BC functionality. The BC architecture provides a high degree of flexibility and autonomy by providing message schedule control, minimizing host overhead for asynchronous message insertion, facilitating bulk data transfers, double buffering, message retry, bus switching strategies, data logging, and fault reporting. The RT architecture provides flexibility in meeting all MIL-STD-1553B protocols. The card includes a message monitor mode and a combined RT/MT mode where the MT will monitor all 1553 communications on the bus including the 1553 channel's assigned RT addresses. The Bus Monitor mode provides complete error detection on 100% fully loaded buses. The Monitor can record data in an industry standard IRIG-106 Chapter 10 format and DMA this data over to the host. This allows for super-low CPU and PCI utilization which can be a critical aspect of embedded systems.

### COTS Solution

- Conduction or Air Cooled PMC
- Front or Rear I/O
- 32-bit, 33/66 MHz PCI Local Bus
- 48-bits, 1 microsecond Time Stamp
- 1 to 8 Dual Redundant MIL-STD-1553 Channels
- 1 MB RAM with Parity per 1553 Channel
- Transformer Coupled Channels
- BC/RT/MT/RTMT Operating Modes
- User-Definable Interrupts
- 8 Avionics (+35V) Discrete I/O
- 8 Digital Discrete I/O

### Bus Controller

- Control/Status Blocks for Individual Messages
- Minor and Major Frame Scheduling to Control Timing of 1553 Messages
- High and Low Priority Asynchronous Message Insertion
- Modify Messages or Data While BC is Running
- Conditional Messages or Subroutines Based on User Defined Conditions
- Multiple BC Retry Programmable Options
- Fully User-Definable Interrupts
- Error Detection as per MIL-STD-1553 Standard

### Remote Terminal

- Choice of Sub-Address Single Message, Double Buffering, Circular Buffering or Global Circular Buffering
- Programmable Interrupt Conditions
- Stack with Descriptors for Individual Messages
- Message Status, Time Tag, Command Word, Data Words
- Programmable Command Illegalization
- Programmable Busy by Sub-Address
- Programmable RT Address via Hardware Connector or Software

## AVIONICS DISCRETE I/O's

The BU-65578F/M card includes eight Avionic Level Discrete I/O Channels that are individually programmable as inputs or outputs. As outputs they are Open-Drain type drivers. When used as inputs these channels are configured to sense Ground / Open discrete inputs with +35V input voltage tolerance. The following specifications apply to these signals: VIL max = 3.5V, VIH min = 4.0V, VOL max = 0.5V. Note that for the -M version the Avionics I/O channels 3-8 also function as RT address inputs for 1553 channel #1. Avionics I/O channels are limited to 0.5A capability.

### DIGITAL DISCRETE I/O's

Up to eight Digital Discrete I/O's pins are individually programmable to be either an output with wraparound or input-only digital discrete. Digital discrete inputs are +5V tolerant and outputs are +3.3V with 1.6mA minimum drive capability.

### Bus Monitor

- IRIG-106 Chapter 10 Compatibility
- On Board DMA Engine for low CPU/PCI Utilization
- Filter Based on RT Address, T/R bit, Sub-Address
- Message Status, Time Tag, Command Word, Data Words
- Programmable Interrupt Conditions
- Simultaneous RT/Message Monitor Option

### Discrete I/O

- 8 +35 Volt Avionics Discrete I/O's
  - Outputs are Low Side Open Collector Drives Capable of Sinking up to 1A
  - Inputs are +35V Tolerant
- 8 Digital Discrete I/O's
  - Outputs are +3.3V with 1.6mA minimum Drive Capability
  - Inputs are +5V Tolerant

### Built In Self-Test Capability

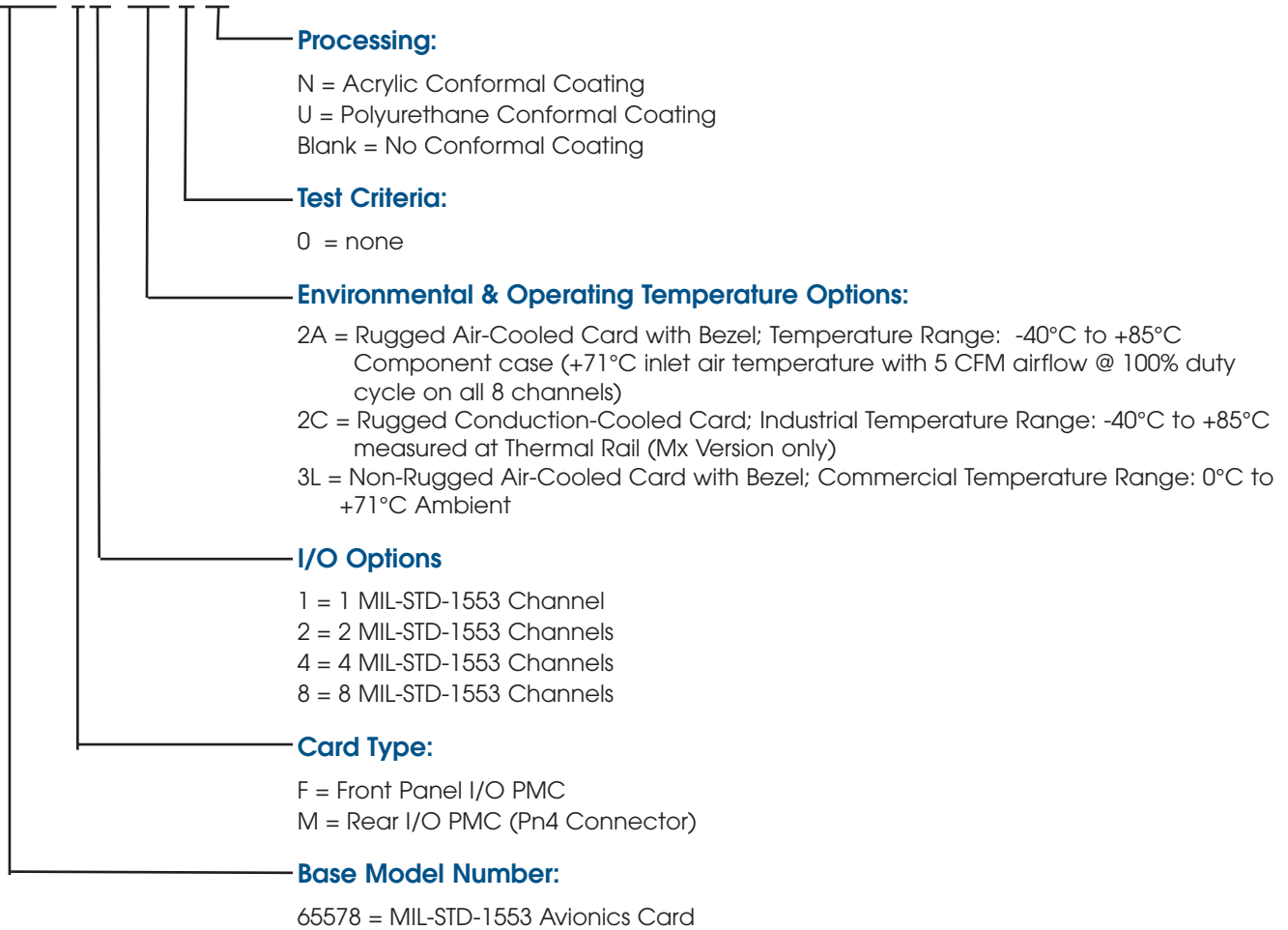
- RAM Self Test
- Register Self Test
- Interrupt Self Test

### Supporting Software

- VxWorks Driver
  - Designed for Wind River's Version 5.x and 6.x
  - Version for Power PC and x86
- Linux Driver
  - Loadable Linux Kernel Version 2.6.x Driver Modules
  - Version for Power PC and x86
- Windows Driver
  - Plug and Play Device Driver for Windows 2000/XP
- High Level MIL-STD-1553 EMACE Plus C SDK

# ORDERING INFORMATION

## BU-65578 FX- 2X 0 X



**Note:**  
 This product contains tin-lead solder.

### Included Software:

**BU-69092SX MIL-STD-1553 EMACE Plus C Software Development Kit**

- 0 = Windows 2000/XP
- 1 = Linux
- 2 = VxWorks

**Optional Front Panel Cable: DDC-75767-X Front Panel Cable**

- 1 = Cable for F8 version
- 2 = Cable for F4 version
- 3 = Cable for F1 or F2 version

STANDARD DDC PROCESSING FOR DISCRETE MODULES/PC BOARD ASSEMBLIES		
TEST	METHOD(S)	CONDITION(S)
INSPECTION / WORKMANSHIP	IPC-A-610	Class 3
ELECTRICAL TEST	DDC ATP	—

The information in this **Data Sheet** is believed to be accurate; however, no responsibility is assumed by Data Device Corporation for its use, and no license or rights are granted by implication or otherwise in connection therewith. Specifications are subject to change without notice.



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